Welcome!

Dear Friends of MicroTCA,

With more than 190 participants from 17 countries, the series of annual MicroTCA workshops at DESY is still going strong. Now in its 8th year, we feel lucky to host such an event of international importance and are grateful to all contributors, especially our industry partners, speakers and exhibitors. We also welcome the continued initiative and support of PICMG.

We have filled the familiar structure of the workshop (tutorials, keynotes, short presentations, an industry exhibition and a poster session) with brand-new content – your contributions regarding the latest MicroTCA developments in labs, research institutions and industrial facilities around the world. There will be lots to talk about, so we have left plenty of room for informal exchange to help you catch up. Many of you have vivid memories of last year's conference dinner, which we conveniently combined with a little cruise through Hamburg harbour. Good news: we will do it again. Ship ahoy!

On a more solemn note, we mourn the passing of Vollrath Dirksen of N.A.T. GmbH. Vollrath had been a towering figure in the world of MicroTCA for many years, always contributing towards the improvement of the standard and its further adoption worldwide. Kind, knowledgeable and very generous with his time and advice, he is greatly missed by everyone who knew him.

The *Future of MicroTCA* has been the subject of many discussions in 2019, and significant progress has been achieved in form of a new *Statement of Work*, heralding the official formation of working groups under the auspices of PICMG. Topics of interest include a new power module definition that will accommodate the requirements of next-generation AMC cards as well as a novel concept to overcome current internal bandwidth limitations. You are very welcome to join the discussion and contribute your own thoughts, experiences and ideas.

This year also saw the first major event featuring MicroTCA in China, complete with keynotes, tutorials, conference-style contributions and many opportunities for exchange with representatives from local facilities like CSNS, IHEP, IMP, NSRL and SARI. We are delighted to meet you again here at our workshop! There are lots of lucky numbers in Chinese culture, and we have learned that *8* is the luckiest of them all, with positive connotations of good fortune, wealth and prosperity. With this in mind, I welcome everyone to the *8th* MicroTCA Workshop on behalf of the organising committee and wish you every success with your current and future projects.

Happy networking!

Dr. Thomas Walter — Hamburg, December 2019

Head of MicroTCA Technology Lab

Chair and Advisory Committee:

Kay Rehlich (Chair)	DESY
Holger Schlarb (Chair)	DESY
Henrik Carling	ESS
Tobias Hoffmann	GSI
Thomas Holzapfel	powerBridge
Christian Ganninger	nVent - Schroff
Matthias Kirsch	Struck
Heiko Koerte	N.A.T.
Ray Larsen	SLAC
Rong Liu	Beijing DAQ Technology Co. Ltd
Dariusz Makowski	Lodz University of Technology
Charles Roberts	ORNL
Fumihiko Tamura	J-PARC Center, Japan
Axel Winter	MPI Plasmaphysik

Local Organising Committee:

Thomas Walter	DESY
Hanna Kunze	DESY

General Information

Venue

DESY CFEL, Building 99, Deutsches Elektronen-Synchrotron, Notkestraße 85, 22607 Hamburg

W-LAN

WLAN name: **MTCA Workshop**
WPA/WPA2-PSK: **ohv3aiFi4eJ4**

Meals

Breakfast:
The DESY cafeteria (building 9, open from 7 a.m.) provides breakfast at your own expenses.
Lunch:
A small lunch will be offered during the workshop in the CFEL building.

Restaurants

Café CFEL (within the CFEL building)
Mo-Fri 8 a.m. to 4 p.m. (very crowded at lunch time)

DESY Canteen & Cafeteria (building 9)
Cafeteria opens Mo-Fri 7 a.m.-11 p.m.(Lunch 11 a.m.-2 p.m.)
Today's menu under https://desy.myalsterfood.de/

Restaurant l'incontro il bistro
Ebertallee 232, 22607 Hamburg. Small restaurant serving Italian food, can be reached on foot from DESY campus

Restaurant Le Jardin
(Mercure Hotel Hamburg am Volkspark) Regional and international food served all day.

Stadtbäckerei Junge
Osdorfer Weg 106, open 6:30 a.m.-6 p.m., bakery serving warm and cold food, exit DESY campus at the main entrance and walk on straight (Zum Hünengrab). At Osdorfer Landstraße turn left, the bakery is within sight.

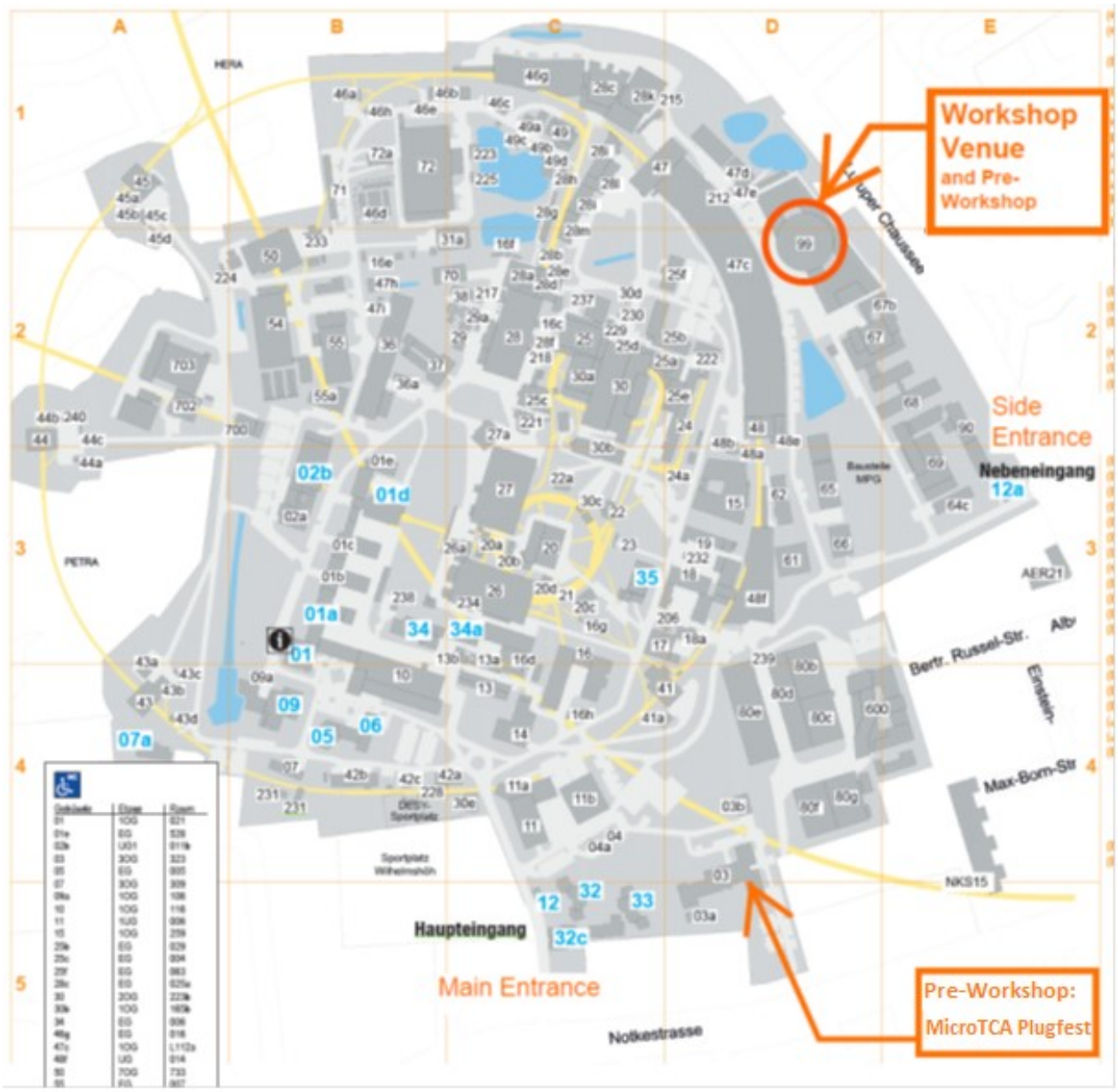
Other useful information

Shopping at the Elbe Einkaufszentrum:
Shopping mall with more than 170 shops, opening hours 09:00 – 20:00. From main gate at Notkestrasse bus no. 1, direction Schenefelder Holt, S Blankenese, Sieversstücken, exit "Elbe Einkaufszentrum".

Supermarket:
LIDL: from main gate at Notkestrasse turn right and walk some 700-800 m down Notkestrasse, LIDL will be clearly visible on the left side of the street at the next junction.

Cashpoint
You will find an ATM in the DESY canteen entrance area in building 9.

Workshop Venue at DESY



Workshop Dinner on “MS Hanseatic”

4th December, 7.30 p.m. – 10.30 p.m.
Boat departure: 7.30 p.m., Überseebrücke Hamburg

The workshop dinner will take place on the MS Hanseatic. We will take dinner while cruising in Hamburg’s famous harbour. The ship departs from Überseebrücke (20459 Hamburg) at 7.30 pm and returns at 10.30 pm.

We provide three shuttle busses starting at 6:30 pm in front of the CFEL. The shuttle busses will return to DESY after the dinner.

If you are not taking the bus shuttle, please make sure to be at Überseebrücke at 7:15 p.m..

Public transport information: Leave DESY at the side entrance. Take bus line 3 from “Luruper Chaussee (DESY)“ to “U Feldstraße”, then U3 to “Baumwall”. The trip takes about 35 minutes.

DESY tours

We offer three DESY tours, organized by the MSK group of DESY. The tours will show you around on the DESY campus and cover the facilities AMTF and FLASH.

Tour 1: Wed, 4 Dec, 12:30 – 13:30

Tour 2: Thurs, 5 Dec, 12:30 – 13:30

Tour 3: Thurs, 5 Dec, 13:00 – 14:00

Meeting point for the tours: Registration desk in the CFEL foyer.

Workshop Programme

Tuesday, 3 December 2019

09:00 - 17:00	**Pre-Workhop**
09:30 - 12:00	MicroTCA Plugfest *Building 3, BAH1*
10:30 - 12:00	Signal Integrity *CFEL*
12:00 - 13:00	**Lunch**
13:00 - 15:00	MicroTCA Tutorial for Beginners *CFEL*
13:30 - 15:00	DMA over PCIe with FPGA *CFEL*
15:00 - 15:30	**Coffee Break**
15:30 - 17:00	Machine Protection in MicroTCA *CFEL*
15:30 - 17:00	Introduction to ChimeraTK *CFEL*

Wednesday, 4 December 2019

CFEL, SR I-III

08:30 - 09:00 **Registration**

09:00 - 09:20 **Welcome** Dr**.** Wim Leemans (DESY)

09:20 - 09:40 **Introduction** Dr. Holger Schlarb (DESY)

09:40 - 10:30 **Session 1, Chair: Holger Schlarb** (DESY)

- PICMG - 25 Years of Open Specifications for Embedded Computing
  Jessica Isquith (PICMG)
- Status of the MicroTCA-based Accelerator Control Systems at the European XFEL and FLASH
  Tim Wilksen (DESY)
- Status of ESS
  Timo Korhonen (ESS)

10:30 - 11:00 **Coffee Break**

11:00 - 12:30 **Session 2: Facility status reports, Chair: Tobias Hoffmann** (Helmholtzzentrum für Schwerionenforschung GSI)

- **Keynote:** Fusion Research with MicroTCA applications
  Axel Winter (MPI Plasmaphysik)
- Summary of MTCA/ATCA workshop in China
  Xinpeng Ma (Institute of High Energy Physics, Chinese Academy of Sciences)
- Survey on perceived strengths and weaknesses of MicroTCA.4
  Daniel Tavares (LNLS)
- MTCA is spreading in accelerator facilities in Japan
  Fumihiko Tamura (J-PARC Center, Japan Atomic Energy Agency)
- mini-CBM data acquisition system - status and outlook
  David Emschermann (GSI Helmholtzzentrum f. Schwerionenforschung)

12:30 - 14:00 **Lunch**

12:30 - 13:30 **DESY Tour 1**

Start of the tour at the registration desk, CFEL, please be on time!

14:00 - 15:45 **Session 3: Products presentations, Chair: Dariusz Makowski** (Lodz University of Technology)

- Industrial high performance computing devices
  Jens Stapelfeld (Xilinx)
- MTCA goes industry
  Friedrich Fix (PowerBridge)
- The diversity of MTCA
  Tim Dally (PowerBridge)
- MTCA.4 Applications for Accelerators: Machine Protection System and Photon Beam Stabilization Exploiting DAMC-FMC25
  Paolo Scarbolo (CAENels)
- Available MTCA.4 Crates and their Backplane Topologies
  Christian Ganninger (nVent- Schroff)
- DAMC-FMC2ZUP a MPSoC based FMC+ carrier card
  Simone Farina (DESY)

15:45 - 16:15 **Coffee Break & Posters**

16:15 - 18:00 **Session 4**: **Future of MicroTCA, Chair: Christian Ganninger** (nVent - Schroff)

- MicroTCA Next Generation: Plans for the Future
  Kay Rehlich (DESY)
- Teledyne e2v, multi GSPS ADC/DAC roadmap
  Jens Michaelsen (Avnet Silica)
- From 40G to 100G - a new MCH concept
  Heiko Körte (N.A.T.)
- Trends that are Influencing Intel Processor-based AdvancedMCs
  Paul Prictoe (Concurrent Technologies Plc)
- A new Zone 3 Class for RF Signals up to 3 GHz in MicroTCA.4
  Johannes Zink (DESY)
- Overview of MicroTCA Techology Lab activities
  Jan Marjanovic (DESY)
- An update on the applications of MTCA in photon science
  Martin Tolkiehn (DESY)

18:30 Transfer from CFEL entrance to Überseebrücke

19:30- 22:30 **Workshop Dinner**

22:30 Transfer from Überseebrücke to DESY main entrance

Thursday, 5 December 2019

CFEL, SR I-III

09:00 - 10:30 Session 5: Subsystems, Chair: Heiko Körte (N.A.T.)

- MTCA-based BPM system design
  Yu Liang (National Synchrotron Radiation Laboratory,USTC)
- Overview of DMCS Projects and MicroTCA.4 Developments
  Dariusz Makowski (Lodz University of Technology)
- MTCA.4-based Button and Strip-Line BPM Electronocs at DESY
  Hans-Thomas Duhme (DESY)
- A MicroTCA-based Design for HEPS Global Timing System
  Fang Liu (Institute of High Energy Physics)
- Insight on failures of MTCA systems installed in FLASH and EuXFEL tunnels
  Julien Branlard , Christian Schmidt (DESY)
- Magnetic and Radiation Field Compatibility of MTCA and PXIe-based Instrumentation
  Stefan Simrock (ITER)

10:30 - 11:00 Coffee Break & Posters

11:00 - 12:30 Session 6: FPGA, Chair: Thomas Holzapfel (PowerBridge)

- **Keynote:** RFSoC, high-performance data processing devices with multi GSPS ADC/DAC
  Jens Michaelsen (Avnet Silica), Michael Oelmann (Xilinx)
- IRIO-OpenCL: Simplified development and integration of DAQ and processing systems using OpenCL for IntelFPGA devices
  Miguel Astrain (Universidad Politecnica de Madrid)
- Certification and improvements of MicroTCA Technology Lab's GigE Vision Stack
  Sven Stubbe (DESY)
- Modernization of MicroTCA.4 FPGA Firmware Framework
  Cagil Guemues (DESY)
- FPGA Configuration and Monitoring via Ethernet in MicroTCA
  Nuno Gonçalves (Universidade de Lisboa, XFEL GmbH)

12:30 - 14:00 Lunch

12:30 - 13:30 DESY Tour 2

13:00 - 14:00 DESY Tour 3

The tour starts at the registration desk, please be on time!

14:00 - 16:10 Session 7: Facility Status Reports, Chair: Axel Winter (MPI Plasmaphysik)

- Overview and experience related to MicroTCA applications at the European XFEL Experiments
  Bruno Fernandes (European XFEL)
- Firmware and software synchronization for MicroTCA roll-out in the LLRF at CERN
  Maciej Suminski (CERN)
- ALBA DLLRF using commercial uTCA platform
  Angela Salom (ALBA)
- Overview of the MYRRHA project and its LLRF MTCA developments
  Wouter De Cock (SCK-CEN)
- Development of MTCA.4-Based LLRF System at SSRF
  Junqiang Zhang (Shanghai Advanced Research Institute,CAS)
- Influences for the cooling performance of a MTCA.4 Crate
  Ralf Waldt (nVent Schroff GmbH)
- Device error handling in ChimeraTK
  Martin Killenberg (DESY)
- Redundant CPU on MTCA System with PCI Express Non-Transparent Bridge
  Ludwig Petrosyan (DESY)
- Closeout
  Holger Schlarb (DESY)

16:10- 16:40 Coffee

Table of Contents

Session 1 14

PICMG - 25 Years of Open Specifications for Embedded Computing 14

Status of the MicroTCA-based Accelerator Control Systems at the European XFEL and FLASH 14

Status of ESS 15

Session 2: Facility status reports 16

Keynote: Fusion Research with MicroTCA applications 16

Summary of MTCA/ATCA workshop in China 16

Survey on perceived strengths and weaknesses of MicroTCA.4 17

MTCA is spreading in accelerator facilities in Japan 17

mini-CBM data acquisition system - status and outlook 18

Session 3: Products presentations 19

Keynote: Industrial high performance computing devices 19

MTCA goes industry 19

The diversity of MTCA 19

MTCA.4 Applications for Accelerators: Machine Protection System and Photon Beam Stabilization Exploiting DAMC-FMC25 20

Available MTCA.4 Crates and their Backplane Topologies 20

DAMC-FMC2ZUP a MPSoC based FMC+ carrier card 21

Session 4: Future of MicroTCA 22

MicroTCA Next Generation: Plans for the Future 22

Teledyne e2v, multi GSPS ADC/DAC roadmap 22

From 40G to 100G - a new MCH concept 22

Trends that are Influencing Intel Processor based AdvancedMCs 23

A new Zone 3 Class for RF Signals up to 3 GHz in MicroTCA.4 23

Overview of MicroTCA Techology Lab activities 24

An update on the applications of MTCA in photon science 24

Session 5: Subsystems 25

MTCA based BPM system design 25

Overview of DMCS Projects and MicroTCA.4 Developments 25

MTCA.4-Based Button and Strip-Line BPM Electronics at DESY 26

A MicroTCA-Based Design for HEPS Global Timing System 26

Insight on failures of MTCA systems installed in FLASH and EuXFEL tunnels 27

Magnetic and Radiation Field Compatibility of MTCA and PXIe-based Instrumentation 27
Session 6: FPGA 28
Keynote: RFSoC, high performance data processing devices with multi GSPS ADC/DAC 28
IRIO-OpenCL: Simplified development and integration of DAQ and processing systems using OpenCL for IntelFPGA devices 28
Certification and improvements of MicroTCA Technology Lab's GigE Vision Stack 29
Modernization of MicroTCA.4 FPGA Firmware Framework 30
FPGA Configuration and Monitoring via Ethernet in MicroTCA 30
Session 7: Facility Status Reports 31
Overview and experience related to MicroTCA applications at the European XFEL Experiments 31
Firmware and software synchronization for MicroTCA roll-out in the LLRF at CERN 32
ALBA DLLRF using commercial uTCA platform 32
Overview of the MYRRHA project and its LLRF MTCA developments 33
Development of MTCA.4-Based LLRF System at SSRF 33
Influences for the cooling performance of a MTCA.4 Crate 33
Device error handling in ChimeraTK 34
Redundant CPU on MTCA System with PCI Express Non-Transparent Bridge 34
Ludwig Petrosyan 34
Poster Abstracts 35
The new revision of the MicroTCA.4-based 8 Channel, Direct Sampling, Single Channel Up-Converter Board 35
Precision X-band RF control system 35
DAQ system for energy dispersive gamma and X-ray detectors 36
Investigation of MTCA power supply problem after power glitch 36
Future perspectives for LLRF Systems in MicroTCA 37
Status and preliminary Test of LLRF System for the MESA Project 37
Status of MicroTCA Implementations at the Spallation Neutron Source 38
MicroTCA Technology Lab (A Helmholtz Innovation Lab): A Status Update on Current Activities 39
DESY MMC System on Module and its application on a low-cost FMC carrier 39

Session 1

PICMG - 25 Years of Open Specifications for Embedded Computing

Jessica Isquith

PICMG

PICMG is a nonprofit consortium of companies and organizations that collaboratively develop open standards for high performance embedded computing applications, including MicroTCA. This presentation will review the 25 years of open specifications that have resulted from the work of hundreds of member companies.

We will discuss the current specifications, our development processes, and the value of PICMG membership. PICMG members benefit by participating in standards development, gaining early access to critical technology, and developing relationships with thought leaders and suppliers in the industry.

Status of the MicroTCA-based Accelerator Control Systems at the European XFEL and FLASH

Tim Wilksen

DESY

MicroTCA-based accelerator controls are nowadays widely used at the European XFEL and the FLASH facility. A brief review of the current status and some experiences with focus on the used MicroTCA technology will be shared. It was one of the key ingredients in the design of the accelerator controls for the European XFEL to use generalized solutions. Many of these now can be utilized for new projects at DESY and have been already implemented at accelerator research facilities and experiments at DESY. An overview of new MicroTCA-based accelerator controls projects and related projects at DESY will be presented.

Status of ESS

Timo Korhonen

ESS

Construction at ESS is proceeding. Commissioning of the first substantial section, the normal conducting Linac, is approaching. The talk gives an outline of the status of the control system preparations, concentrating on the MTCA-based systems. An overview of the developments and the control system architecture is given. Some results of newly developed applications are presented.

Session 2: Facility status reports

Keynote: Fusion Research with MicroTCA applications

Axel Winter

MPI Plasmaphysik

This presentation will provide an overview of the usage of MicroTCA systems at nuclear fusion facilities around the world. Many DAQ systems for fusion diagnostics at KSTAR (Daejeon, Korea) and Wendelstein 7-X (Greifswald, Germany) are currently based on the MicroTCA standard and their numbers are growing steadily. Also ITER, the next generation Tokamak, has committed to support MicroTCA as part of their DAQ portfolio. After a brief overview about nuclear fusion in general and typical diagnostic challenges, this talk will highlight a number of examples for existing MicroTCA-based systems and also provide an outlook regarding the future plans for MicroTCA at those facilities.

Summary of MTCA/ATCA workshop in China

Xinpeng Ma

Institute of High Energy Physics, Chinese Academy of Sciences

Summary of the MTCA/ATCA workshop for research and industry at IHEP China in June 2018 is shown and future plans are also presented.

Survey on perceived strengths and weaknesses of MicroTCA.4

Daniel Tavares

LNLS

More and more scientific facilities have been adopting MicroTCA.4 as the standard for new electronics. Despite the advertised advantages in terms of system manageability, high availability, backplane performance and supply of high quality COTS modules by industry, the standard still lacks a greater acceptance in the accelerators community. This contribution will report on a survey carried out among the MicroTCA.4 adopters in the accelerator community to probe the perceived strengths and weaknesses of the standard and its ecosystem at present days.

MTCA is spreading in accelerator facilities in Japan

Fumihiko Tamura

J-PARC Center, Japan Atomic Energy Agency

The application of MTCA for accelerators was pioneered by KEK.
Although the development of the LLRF with MTCA at KEK was successful, it took time for the other accelerator facilities to employ MTCA-based systems. In these years, several applications of MTCA in Japan have been reported. The next-generation LLRF control system for the J-PARC RCS based on MTCA.4 was successfully deployed.
A new MTCA-based LLRF system for an ion synchrotron is under development at WERC.
There are more applications. The status of the application of MTCA in the Japanese accelerators and the future perspective are presented.

mini-CBM data acquisition system - status and outlook

David Emschermann

GSI Helmholtzzentrum f. Schwerionenforschung

The Compressed Baryonic Matter experiment (CBM) will be based at the new Facility for Antiproton and Ion Research (FAIR), which will deliver heavy-ion beams up to energies of 14 AGeV for N=Z beams. In nucleus-nucleus collisions at these beam energies strongly interacting matter with densities up to 10 times normal nuclear matter is expected to be produced. The key objective of CBM is to investigate the QCD phase diagram in the region of high baryon-densities, where a first order phase transition from hadronic to partonic matter as well as a chiral phase transition is expected to occur, representing a substantial discovery potential at FAIR energies. As a fixed-target experiment CBM is consequently designed to cope with very high interaction rates up to 10 MHz. This will allow to perform high precision measurements of extremely rare probes which have not been accessible by previous nucleus-nucleus experiments in this energy regime. To achieve the high rate capability CBM will be equipped with fast and radiation hard detectors employing free-streaming and self-triggered readout electronics.

The newly built mini-CBM (mCBM) setup at GSI serves as technology demonstrator for the full CBM experiment. A prototype high performance Data Acquisition (DAQ) system for mCBM was built in 2018. In spring 2019 mCBM took first beam for a high rate system test of the detector systems, the free-streaming readout chain, the online time-slice building and online data monitoring in the First Level Event Selector (FLES). We will report on the current status of the mCBM DAQ system, which is based on microTCA hardware.

Session 3: Products presentations

Keynote: Industrial high performance computing devices

Jens Stapelfeld

Xilinx

Xilinx Roadmap and Tool setup

- Alveo, high performance computing
- Vitis, unified development tools
- Versal, heterogeneous computing devices

MTCA goes industry

Friedrich Fix

PowerBridge

The most convincing feature of an MTCA system are its multiple uses.
With the same basic system and different AMCs, almost all requirements in the industry can be met. Representing all industrial applications, this presentation only shows applications in image processing and communication.

The diversity of MTCA

Tim Dally

PowerBridge

MTCA offers a variety of uses for various applications such as accelerator control systems, medical beam diagnostics, video conferencing, image processing, and more.

The wide selection and availability of AMC processors and peripheral cards allows us to build MTCA systems for every customer application.

This presentation shows suitable solutions for applications based on examples of communication technology and image processing.

That's why we call MTCA: Universal Data Acquisition Computing System (UDAC).

MTCA.4 Applications for Accelerators: Machine Protection System and Photon Beam Stabilization Exploiting DAMC-FMC25

Paolo Scarbolo

CAENels

This contribution aims to show how MTCA.4 is used for the development of accelerator systems for diagnostics and photon beam stabilization exploiting the DAMC-FMC25 AMC carrier board features.

We present the system architecture, the final application and some preliminary results regarding a Machine Protection System (MPS) and an Electron Beam Stabilization System (PBSS) in research facilities.

The MPS is composed by a third-party control board that communicates with multiple AMC-PICO-8 8-channel picoammeters developed by CAEN ELS. The AMC-PICO-8 stores acquired data buffer up to 1 Msps, generates a MPS signal upon specific over-threshold conditions and stops the acquisition after a post-mortem signal.

The PBSS elaborates the information received from a position detector via the FMC-PICO-1M4 picoammeter front-end, performs the feedback controller computations (IIR filter) and sends the correction signals directly to the FAST-PS power supplies equipped with fast low-latency SFP interfaces.

The communications with backplane (PCIe) and FMC modules (SPI) and all the high demanding computations are handled by the FPGA available on the DAMC-FMC25.

Available MTCA.4 Crates and their Backplane Topologies

Christian Ganninger

nVent Schroff

This presentation gives an overview of the nVent SCHROFF Standard MTCA.4 Crate solutions and the various backplane topologies, showing the different cooling concepts, slot orientations and arrangements and system features as well as additional backplane connectivities. Furthermore a short outlook of the upcoming Crate solutions will be presented.

DAMC-FMC2ZUP a MPSoC based FMC+ carrier card

Simone Farina

DESY

The ecosystem of FMC/FMC+ carriers in MicroTCA (Advanced Mezzanine Card form factor) is very diverse. The requirements for such a board are very demanding, sometimes even opposing to each other, and the definition of a specification that will satisfy most of the use cases without crossing the boundary of the 80W available for an AMC card is a challenging task.

Presented here is the DAMC-FMC2ZUP, a modern and high-performance FMC+ carrier in AMC form factor, which hosts a Xilinx Zynq UltraScale+ MPSoC. The FPGA has a total of 52 transceivers (32 GTH, 16 GTY, 4 GTR) providing support to the diverse communication interfaces towards the FMC slots, backplane and RTM. The four cores ARM-A53 processor with Mali graphics and the availability of DisplayPort and USB interfaces over the USB type-C connector allows to use this board as a replacement to an additional CPU card for not so high demanding applications.

The availability of an independent dual core ARM-R5 that is certified for safety critical applications allows the user to implement either or both real-time and safety related applications.

The design supports different methods of synchronization to an external timing system and already includes all the necessary electronics to implement a White Rabbit endpoint when paired with the external SFP breakout board.

DAMC-FMC2ZUP is a versatile platform ideal to perform control tasks around a particle accelerator. Combined with the modularity of the MicroTCA platform it can be a building block for a larger system.

The discussion will be concluded with an overview of possible approaches to overcome the power limitations in the future.

Session 4: Future of MicroTCA

MicroTCA Next Generation: Plans for the Future

Kay Rehlich

DESY

The next generation of CPUs will support PCIe gen 5. And to allow faster CPUs more power is required for AMCs. To address these challenges a new PICMG working group is in preparation. Goals and options to keep MicroTCA as a leading standard will be presented.

Teledyne e2v, multi GSPS ADC/DAC roadmap

Jens Michaelsen

Avnet Silica

Teledyne e2v product Roadmap and Tool setup

- ADC, up to 6.4 Gsps
- DAC, up to 8 Gsps
- ESIstream, resource optimized ADC/DAC protocol

From 40G to 100G - a new MCH concept

Heiko Körte

N.A.T.

Increasing demands for modularity and bandwidth create a constant challenge to meet the requirements of application from the “low end” (i.e. Industrial IoT) to the “high end” (i.e. data processing with high-end FPGAs). Therefore, in the long term a new concept for the MicroTCA Carrier Hub (MCH) is needed which allows a flexible mix-and-match of MCH sub-modules and provides state-of-the art switching technology for slim and fat-pipe fabrics at the same time. The presentation will show how this transition from existing MCHs to future solutions can be smoothly effected while maintaining a maximum on backward compatibility.

Trends that are Influencing Intel Processor based AdvancedMCs

Paul Prictoe

Concurrent Technologies Plc

Historically, an Intel processor based AdvancedMC module was used as the central control station in a MicroTCA system to display status information, provide local storage and to act as a gateway between the other boards in the system and the outside world via a network connection. That's an important function and has become elevated as this board typically can act as the root of trust in a system. To do that we include a variety of security technologies and features that should be of interest given the sensitive nature that the products are controlling.

In addition, more users are using compute intensive Intel processor based AdvancedMCs for local data processing. Whilst Intel CPU only solutions offer significantly less processing capability compared to GPU and FPGA based solutions, they are much easier to program and by using Intel's OneAPI, it is possible to add co-processors like FPGA without code changes. In this type of heterogeneous scenario, OneAPI will optimise the code to use the available processing resources in a similar way to that of OpenVINO which is specific to Artificial Intelligence and Inference at the Edge applications.

A new Zone 3 Class for RF Signals up to 3 GHz in MicroTCA.4

Johannes Zink

DESY

In MicroTCA.4 the connection between AMC and RTM is realized with a differential pair connector. Transporting high frequency analog signals (> 300 MHz) over the differential pair connector leads to intense crosstalk between the differential channels.

A new type of Zone 3 connection is needed, capable of transporting signals up to 3 GHz. The new analog Zone3 class RF1.0 based on single-ended coaxial connectors will be presented. First measurement data from several evaluation boards showing the single-ended performance and isolation of the new coaxial connectors will also be presented. The class RF1.0 can be used for direct sampling application feeding RF signals from the RTM to the AMC side or for RF sampling DAC applications in the opposite direction.

Overview of MicroTCA Techology Lab activities

Jan Marjanovic

DESY

In its second year of operation has MicroTCA Technology Lab continued to foster the MicroTCA community and deliver customer-oriented solutions. We observe that the MicroTCA market is growing and more and more institutes are adopting or considering adopting MicroTCA as a platform for future installations.

We present here the projects where MicroTCA Technology Lab was involved last year. To name a few: we have successfully delivered turn-key LLRF systems, certified our GigE Vision FPGA implementation and enhanced it with 10 Gigabit Ethernet version, developed a new Zone 3 class for high-frequency RF signals, productized our MMC implementation in DMMC-STAMP and developed a Zynq UltraScale+ MPSoC-based FMC+ carrier. We have also rethought and redesigned MTCA training courses, to give them more emphasis on the needs of the experimental physics.

Together with our colleagues from IHEP we have organized the first MicroTCA Workshop in China, and we are determined to continue this tradition also in the years to come. We have also participated at several conferences and organized several single-day events.

We conclude this overview with a brief summary of the upcoming projects.

An update on the applications of MTCA in photon science

Martin Tolkiehn

DESY

In my talk I will present new applications of MTCA at beamline P24 including the TCK7 based camera readout system, the planned beam stabilization system and the status of the MTCA motor controller project.

Session 5: Subsystems

MTCA based BPM system design

Yu Liang

National Synchrotron Radiation Laboratory, USTC

A digital beam position measurement system based on MTCA.4 is designed. The system includes a RF front-end circuit and a digital signal processing module. The RF front-end circuit adjusts the signals from the beam position detectors to meet the requirements of the analog to digital converter. The digital signal processing algorithm is implemented in the FPGA. Multi-rate signal decimation, CORDIC algorithm, difference-over-sum algorithm are implemented in the FPGA.Data on demand at Turn-by-Turn (revolution) frequency(TBT data), fast acquisition data(FA data) and slow acquisition data (SA data) are obtained after the digital signal processing in the FPGA. The hardware system is based on MTCA.4 with high integration and reliable performance and the RF front-end gain can be adjusted through the serial port flexibly.

Overview of DMCS Projects and MicroTCA.4 Developments

Dariusz Makowski

Lodz University of Technology

The Lodz University of Technology, Department of Microelectronics and Computer Science is involved in the development of MicroTCA.4 and MicroTCA.4.1 standards from 2007 onwards. Since that time, we developed various MicroTCA.4 components including Intelligent Platform Management, Advanced Mezzanine Cards (AMCs), Rear Transition Modules (RTMs) for data acquisition and processing systems used in numerous accelerators and fusion projects.

The presentation will discuss selected projects ongoing at our department based on MTCA.4 technology.

MTCA.4-Based Button and Strip-Line BPM Electronics at DESY

Hans-Thomas Duhme

DESY

We present a new BPM electronic for button and strip-line monitors based on MTCA.4.

The system is used for Beam position measurement and as an part of an array also for energy measurement.

The electronics are installed at nearly 100 BPMs and EBPMs.

We summarize the recent analog and digital hardware development and operational experience at FLASH, XFEL and PITZ.

A MicroTCA-Based Design for HEPS Global Timing System

Fang Liu

Institute of High Energy Physics

The High Energy Photon Source (HEPS) is a fourth generation synchrotron radiation light source with top electron energy of 6 GeV stored in a 1360-m circumference storage ring and a low emittance of less than 0.06nm·rad which is scheduled to complete its construction by the end of 2025. Because of high precision requirements of storage ring swap-out injection and extraction, the bottom width of the kickers' pulse need to be shorter than the separation between two bunches which is 12ns. Consequently, a high precision global timing system with an accuracy of about 10ps has to be designed and implemented. This talk will outline the MicroTCA based global timing system design and report the progress of the high precision AMC timing receiver in the event-based timing system.

Insight on failures of MTCA systems installed in FLASH and EuXFEL tunnels

Julien Branlard, Christian Schmidt

DESY

FLASH has been operated with MTCA.4-based LLRF systems since 2013 and the European XFEL since 2017. We are now starting to see some failures which could be related to the fact that these systems are placed in a radiation prone environment. This contribution aims at presenting a first insight on the impact of radiation on the MTCA.4 system. In particular, the different shielding types and the different ways of measuring radiation are shown. Correlation between hardware or firmware failures with the measured radiation is presented. Some mitigation strategies are also discussed. Other failures linked to power glitches or loss of pcie communication will also be presented.

Magnetic and Radiation Field Compatibility of MTCA and PXIe-based Instrumentation

Stefan Simrock

ITER

Electronics exposed to magnetic or radiation fields are susceptible to components failures or performance degradation. In 2012 studies of MTCA and PXIe systems have been performed at DESY for magnetic fields and for radiation fields at ENEA, JSI and Atomki. In this presentation the results of these tests will be summarized.

Session 6: FPGA

Keynote: RFSoC, high performance data processing devices with multi GSPS ADC/DAC

Jens Michaelsen, Michael Oelmann

Avnet Silica, Xilinx

Xilinx RFSoC Roadmap and feature set

- Gen 1,2,3, … multi GSPS ADC/DAC SoCs
- Scalability and Migration path
- from 1 to 100 G-Bit Ethernet
- ERNIC/RDMA server offloading

IRIO-OpenCL: Simplified development and integration of DAQ and processing systems using OpenCL for IntelFPGA devices

Miguel Astrain

Universidad Politecnica de Madrid

Many frameworks exist to ease the integration of FPGA based systems into the Instrumentation & Control systems that are required on Big Science facilities. We present a new approach, using the heterogeneous programming language OpenCL to design and develop acquisition and processing applications. This approach reduces the usage of HDL languages significantly to describe the hardware on the FPGA, shortens the development cycle for compliant COTS solutions, and is well suited for the heterogeneous environment that is often found on Big Science experiments.

The work presented here is a set of methods and tools that allow developing applications for FPGA-based instruments in a standardised way. The framework comprises elements such as: an OpenCL compliant Board Support Package with a PCIe interface; an OpenCL IO channel to communicate with high-speed AD/DA converters using the JESD204B standard; a set of OpenCL Kernels to support common DAQ functionality, capable of acquiring and processing at high sampling rates; and a standardized software interface, including the ITER Nominal device Support (NDSv3) software layer that integrates the whole solution with EPICS.

On the hardware side, the system has been implemented in an MTCA chassis with a carrier hub, which provides an optical PCIe (gen3) interface, connected to the host computer. The

Advanced Mezzanine Card (AMC) module is the N.A.T. Advanced Mezzanine Card NAMC-Arria10-FMC . This board mounts an IntelFPGA ARRIA10-SoC and includes an FMC (FPGA Mezzanine Card) connector where the Analog Devices AD-DAQ2FMC-EBZ module is providing two 1GS/s ADC channels together with two 1GS/s DAC channels.

An example use case for data acquisition and processing system was implemented to estimate the average neutron flux emitted by the plasma in a fusion experiment. The DAQ system digitises the pulses produced by the neutrons in the fission chamber and, applies hardware signal processing algorithms to estimate the neutron flux: Pulse Counting, Campbelling and Current counting. All the high-performance tasks of acquiring and processing involved in the algorithms are carried out by OpenCL Kernels, which, as a result of the compilation process, are implemented in hardware that is deployed in the FPGA.

Certification and improvements of MicroTCA Technology Lab's GigE Vision Stack

Sven Stubbe

DESY

The DIPC-7050 GigE Vision Stack is a system solution for running GigE Vision cameras in a FPGA/SoC- based environment. It is usable in wide array of industrial and scientific applications. By integrating the component in their system, users are able to create and run their own high performance image processing solutions without taking care of any camera interfacing; especially without taking care of the GigE Vision standard.

This talk outlines the latest developments and improvements of the DIPC-7050 GigE Vision Stack.

We present the results of the products standard certification at AIA plug-fest, where our implementation had to interface with cameras from several vendors. Our implementation is now officially certified as a GigE Vision compliant product.

For covering the increasing demand of higher data throughput, the GigE Vision standard offers a 10Gigabit Ethernet variant. In the last couple of month we upgraded our solution for operating with devices via 10 Gigabit Ethernet. We present the improved version and discuss the performance.

Modernization of MicroTCA.4 FPGA Firmware Framework

Cagil Guemues

DESY

The MSK group in DESY has been working on a common framework to develop FPGA firmware for MicroTCA standard for over 15 years. This highly modular, abstracted framework has been used to deploy many accelerator facilities inside and outside of DESY. With increasing complexity, maintenance and continuous integration becomes critical in order to ensure minimal downtime for FPGA firmware related failures. This talk gives an overview of the framework as well as future upgrades of interfaces, revision control and continuous integration.

FPGA Configuration and Monitoring via Ethernet in MicroTCA

Nuno Gonçalves

Universidade de Lisboa, XFEL GmbH

In the European XFEL (EuXFEL), the MicroTCA.4 platform hosts Advance Mezzanine Cards (AMCs) with FPGAs for data acquisition, processing and timing distribution. Communication with these devices, configuration, monitoring and raw data receiving and processing, is done via PCI Express (PCIe) using a CPU AMC.

In some setups, FPGAs are not used for data acquisition but transmit information to devices outside of the MicroTCA crate (for example detectors). The FPGA device is configured in the beginning of an experiment and periodically monitored afterwards. In these cases, the CPU's sole function is to provide PCIe communication, increasing the cost and configuration complexity per crate. Since the MCH can also communicate via Gigabit Ethernet with the AMCs of the crate, we can bypass the need for a CPU in the crate by developing an Ethernet protocol to communicate with the FPGAs. In addition, for setups where the data volume is not significant, this communication method can also be used to send raw and process data directly from the MCH to our DAQ system.

In this presentation, we will demonstrate how such communication is being developed in the EuXFEL.

Session 7: Facility Status Reports

Overview and experience related to MicroTCA applications at the European XFEL Experiments

Bruno Fernandes

European XFEL

Since start of user operation two years ago, the European X-Ray Free Electron Laser Facility (European XFEL) is relying on the MicroTCA platform for timing distribution, data processing from large 2D detectors, fast digitization and processing of pulse signals as well as low latency communication protocol for VETO and Machine Protection System. To cope with the experiments that use the generated ultra short coherent X-Ray flashes, spaced by 220 ns and with a duration of less than 100 femtoseconds, almost 40 individual MicroTCA systems are used at the photon beam lines and experiments, all fully integrated in our control and DAQ systems and monitoring solution to immediately identify problems if they occur.

Our experience with the platform grows in parallel with user requests for more particular and challenging case studies and tailo- made hardware algorithms. This requires integration of new hardware and, at the same time, taking advantage of MicroTCA features that where not in use before.

In this presentation, we will provide an overview of the MicroTCA platform in our environment, the results and experiences from last year's experiments, as well as an outlook on future developments.

Firmware and software synchronization for MicroTCA roll-out in the LLRF at CERN

Maciej Suminski

CERN

During the long shutdown from 2019 to 2020, CERN's Super Proton Synchrotron (SPS) is undergoing a comprehensive upgrade of its Low Level RF system, using MicroTCA as a hardware platform.

The new system, currently under development, attempts to maximise firmware reuse by implementing its functionality as independent IP cores, each of which must be supported by corresponding software components which interface it to the accelerator control system. Any changes in the HDL need to be followed consistently by changes in the software layers. This talk will present an overview of the software stack and tools which have been developed to synchronize the firmware and software during the development process.

ALBA DLLRF using commercial uTCA platform

Angela Salom

ALBA

The Digital LLRF of ALBA has been implemented using commercial cPCI boards with Virtex¬4 FPGA, fast ADCs and fast DACs. The firmware of the FPGA is based on IQ demodulation technique and the main feed-back loops adjust the phase and amplitude of the cavity voltage and also the resonance frequency of the cavity. But the evolution of the market is moving towards uTCA technology and due to the interest in this technology by several labs, we have developed at ALBA a DLLRF using a HW platform based on uTCA commercial boards and Virtex¬6 FPGA. Also, a new approach based on commercial AMC boards modified to be used as standalone products has been studied. Stand-alone boards can be a good solution for low budget projects where no interconnections between different modules are needed. This presentation will cover these development and the main differences between them.

Overview of the MYRRHA project and its LLRF MTCA developments

Wouter De Cock

SCK-CEN

This talk will discuss the status of the MYRRHA project with a focus on the current and planned LLRF developments for the first phase of the project.

Development of MTCA.4-Based LLRF System at SSRF

Junqiang Zhang

Shanghai Advanced Research Institute, CAS

Since we got the first MTCA.4 platform in 2014, the MTCA.4-based Low Level RF system has been widely used in many linear accelerators at SSRF. This talk gives an introduction of all accelerator projects, the development of the software and the firmware, and also the performance of the LLRF system.

Influences for the cooling performance of a MTCA.4 Crate

Ralf Waldt

nVent Schroff

A MicroTCA Crate shall be capable to cool 80W per slot under standard conditions. This presentation shows under which circumstances the cooling performance is tested by the crate vendor. Based on real experience it will show how different slot air impedances, air short cuts or air blocks affects the cooling performance of the crate.

Device error handling in ChimeraTK

Martin Killenberg

DESY

ChimeraTK is a tool kit to write application servers for control systems.

When integrating devices into a control system, the device servers usually contain a large fraction of error handling code. Many of these errors are runtime errors which occur when communicating with the hardware. Not only malfunctioning of the hardware can cause these errors, but also a board which is turned off via the hot-plug mechanism in a MicroTCA crate.

We report how ChimeraTK introduces a standardised way to raise and report errors, and to do the re-initialisation when recovering from an error. All this is handled in the framework, which significantly simplifies the business logic because it is not mixed with error handling code any more.

Redundant CPU on MTCA System with PCI Express Non-Transparent Bridge

Ludwig Petrosyan

DESY

One of the main characteristics of any control system is reliability and uninterrupted operation.

Reaching that lofty target, however, requires more than having reliable hardware, hot-swap repair capabilities and robust software design. High availability needs help from many redundant components, including redundant CPUs.

The PCI Express standard is currently the most widely used architecture. The MTCA as well as the majority of architectures today use the PCI Express as a central bus of data transmissions.

To protect against a failing CPU taking the entire system down, a backup CPU can be in place, ready to take over. One method is to have a secondary CPU behind a Non-Transparent Bridge and use Non Transparent Bridge failover sequence.

Our experience of the adjustment, starting and testing as well as use of the Redundant CPU on the MTCA system will be presented.

Poster Abstracts

The new revision of the MicroTCA.4-based 8 Channel, Direct Sampling, Single Channel Up-Converter Board

Uros Mavric

DESY

Extensive measurements of the DRTM-DS8VM1 gave insight into which sections on the module can be further improved. Among all the various features that were tested we present the latest results of AC and DC channels noise spectral densities. Preliminary results of the long-term drift compensation are also presented. Finally, the major changes being implemented on the board are presented.

Precision X-band RF control system

Matthias Reukauff

DESY

The new PolariX TDS and its tomographic capabilities will be used in FLASH2, FLASHForward and SINBAD and shall provide a new level of beam diagnostics. It is developed in cooperation between DESY, PSI and CERN and requires X-band RF front-ends for the measurement of the 12 GHz electric fields. The cavity, waveguide and klystron signals will be down-converted from 12 GHz to 3 GHz and further processed in a standard 3 GHz S-band LLRF system based on MicroTCA.4. We will present the methods used to convert the signals as well as providing an overview of the MicroTCA.4 functions used in this setup. Measurements have shown a short-term jitter of less than 1.5 fs rms added by the conversion system.

DAQ system for energy dispersive gamma and X-ray detectors

Jan Timm

DESY

We present a new data acquisition system for energy dispersive X-ray and gamma detectors based on the MicroTCA.4 standard, which has been developed for photon science applications at DESY's brilliant X-ray source PETRA III.

At the center of this development is a new real-time pulse shape analysis algorithm and trigger system. Due to the noise reducing properties of the algorithm, the data are very clean and a very low threshold value can be achieved. With a previously developed firmware framework we have implemented the new algorithm in the Field Programmable Gate Array (FPGA) of the commercialized SIS8300L card. This ten-channel, fast ADC card was used in conjunction with an amplifier rear transfer module (DRTM-AMP10), developed by the authors and optimized for energy dispersive detectors. In combination with our control software, this data acquisition system offers a high energy resolution of 130 eV FWHM at 5.4 KeV with a peaking time of 560 nanoseconds (measured with an Amptek detector) and supports counting rates of more than 10^6 counts per second and enables continuous data acquisition without conversion time. It provides highly accurate time information for a wide range of detector types up to one clock cycle (8 ns), independent of the deposited energy, thanks to the constant fraction discriminator similar features of the algorithm. In supported file formats such as HDF5 and ROOT, various data is provided, ROI, histogram, extended event information up to the total pulse shape for each event. Thanks to the MicroTCA.4 standard, advanced clocking and triggering as well as high data throughput via PCIe and scalability are possible.

The financial support of the project by the DESY Strategy Fund is recognized.

Investigation of MTCA power supply problem after power glitch

Mariusz Grecki

DESY

During the operation of many MTCA based systems, we noticed problems after power glitches. The presentation reports on investigations of the problem. Thanks to the collaboration with the power supply manufacturer the observed problem with MTCA power supply was solved by a firmware upgrade.

Future perspectives for LLRF Systems in MicroTCA

Frank Ludwig

DESY

In the poster we present the R&D at DESY to enhance the capabilities of future LLRF systems. This includes improvement and performance evaluation of current boards, extensions toward attosecond field receivers and supplementary modules that ease LLRF operations.

Status and preliminary Test of LLRF System for the MESA Project

Jiaoni Bai

Institut für Kernphysik, Johannes Gutenberg-Universität Mainz

The Mainz Energy-recovering Superconducting Accelerator (MESA) is currently under construction at the Institut für Kernphysik (KPH) at Johannes Gutenberg-Universität Mainz. MESA is a multi-turn Energy Recovery Linac (ERL) and aims to serve as user facility for particle physics experiments. The RF-accelerating systems of MESA consist of two cryomodules, each with two 9-cell TESLA superconducting (SC) cavities, and eight normal conducting cavities. They operate in continuous wave (CW) mode. The MicroTCA.4 based digital low-level radio frequency (LLRF) system developed at DESY, Hamburg is adapted for the MESA cavities to guarantee a cavity accelerating field amplitude and phase RMS stabilities of 0.01% and 0.01°.

In this presentation, a LLRF system test with a standalone normal conducting MESA single cell buncher cavity is shown. The amplitude and phase stabilities of the test are 0.05% and 0.05° respectively, which are limited by the stability of the master oscillator of the test bench. Furthermore, the overview of the LLRF system integration into the MESA cryomodules test bench at Helmholtz-Institut Mainz (HIM) test bunker is presented, as well as the preliminary LLRF test results at a temperature of 2 K. The RMS stability requirements are not yet reached due to the lack of the frequency detuning control and the controller parameter optimization. Both are still under development.

Status of MicroTCA Implementations at the Spallation Neutron Source

Eric Breeding, Charles Roberts

Oak RIdge National Laboratory

The Trigger Control, Injection Kicker Waveform Monitor and Ring Low Level RF systems at the Spallation Neutron Source are currently operating with MicroTCA based solutions. MicroTCA based Machine Protection System is installed on segments of the machine and under testing. A 16 channel 2 GS/s coherent sampling Extraction Kicker Waveform Monitor with segmented memory acquisition mode is in early development using MicroTCA. Also, under development using MicroTCA is a safety pedigreed Beam Power Limiting System. This poster will cover those and other MicroTCA efforts at the SNS.

Drift Compensation Measurements of RF Field Detectors operating in CW Mode and based on MicroTCA.4 Standard

L. Butkowski, B. Dursun, C. Guemues, F. Ludwig, U. Mavric, H. Schlarb, C. Schmidt

DESY

The latest drift compensation measurements are presented using the drift-compensation module for CW operation (DCM-CW) of RF field-detectors. The correlation between pilot phase detection on two different channels is studied. The poster summarizes the system settings required for the optimal long-term and short-term performance.

MicroTCA Technology Lab (A Helmholtz Innovation Lab): A Status Update on Current Activities

Thomas Walter, Holger Schlarb, Ilka Mahns

DESY

Helmholtz Innovation Labs (HILs) have been established throughout Germany since 2016 to create *enabling spaces* for the interaction of large public research centers with industry. Possible areas of cooperation include joint product development or improvement, demonstration and test of novel industry solutions and business models, marketing and training as well as supporting activities for ermerging user communities. Within the HIL-framework, DESY has established the *MicroTCA Technology Lab* with the following core activities:

- High-end test and measurement services,
- Customer-specific developments in MicroTCA (hardware, firmware, software),
- Turn-key System configuration and integration.

Officially opened in April 2018, our lab has delivered projects in industry and research in these areas while maintaining links to a wide spectrum of industry partners, supporting the further enhancement of the MicroTCA standard by contributing to development initiatives within the framework provided by PICMG.

DESY MMC System on Module and its application on a low-cost FMC carrier

Michael Fenner

DESY

A complete MMC System-on-Module was developed. It is s a small stamp-sized (25x29x2.3 mm) component which can be mounted on top or bottom side of any AMC card.
The module handles the complete communication to the MCH. For basic operation, the user boards needs virtually no additional components to allow management and power delivery from the system. The SoM is pre-programmed and contains an ARM Cortex-M4 microcontroller and a CPLD.
It provides advanced features such as JTAG arbitration (allows acces from JTAG switch module), in-system programming (via IPMI/HPM) of the module and up to two user FPGAs, PMBUS power management, RTM handling and RTM power delivery.

The Low-Cost Zynq-7000 based FMC Carrier DFMC-FMC1Z7O is based on this MMC module. It contains a

XC7Z030 or XC7Z045 FPGA and 1 GB on-board DDR3 memory. The board is designed for controlling RTMs, offers 48 digtal IOs (selectable 3.3V and 5V I/O) on the front panel and provides an FMC slot for expansion with up to four high-speed transceivers (MGTs) with up to 10Gbps data rate.